Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. - 8. (Canceled)

9. (Currently Amended) A time division multiple access (TDMA) wireless subscriber unit comprising:

a plurality of circuit components, wherein each of the plurality of circuit components is configured to operate in a first signal processing state having an on power consumption level, a second signal processing state having an off power consumption level, and a third signal processing state having an intermediate power consumption level; and

a power interface circuit coupled to the plurality of circuit components, wherein the power interface circuit is configured to provide at least one of the on power consumption level, the off power consumption level, and the intermediate power consumption level, and

wherein at least one of the plurality of circuit components is configured to transition among at least two of the first signal processing state, the second signal processing state, and the third signal processing state based on a time slot of a TDMA frame assigned to the TDMA wireless subscriber unit.

10. (Previously Presented) The TDMA wireless subscriber unit of claim 9, further comprising:

a plurality of clocks, wherein one of the plurality of clocks is selected for one of the plurality of circuit components based on a current one of the first signal processing state, the second signal processing state, and the third signal processing state.

11. (Previously Presented) The TDMA wireless subscriber unit of claim 10, further comprising:

a software controller register coupled to the plurality of circuit components, wherein the software controller register is configured to produce the plurality of clocks.

12. (Previously Presented) The TDMA wireless subscriber unit of claim 9, wherein each circuit component of the plurality of circuit components is further configured to operate in fourth signal processing state including a reduced power sub-state.

13. (Canceled).

14. (Previously Presented) The TDMA wireless subscriber unit of claim 9, wherein one of the plurality of circuit components is configured to retain operating state information to resume processing in response to a transition from the third signal processing state to the first signal processing state.

15. (Previously Presented) The TDMA wireless subscriber unit of claim 9, wherein at least one of the plurality of circuit components is configured to transition from the first signal processing state to either the second signal processing state or the third signal processing state during a call connection.

16. (Previously Presented) The TDMA wireless subscriber unit of claim 9, wherein the plurality of circuit components are configured to be selectively operated in any one of the first signal processing state, the second signal processing state, and the third signal processing state responsive to a radio control channel timeslot to determine the presence of call traffic or a traffic channel assigned to the TDMA wireless subscriber unit.

17. (Canceled)

18. (Previously Presented) The TDMA wireless subscriber unit of claim 9, wherein the at least one of the plurality of circuit components is configured to transition among the first signal processing state, the second signal processing state, and the third signal processing state during a signal time slot.

19. (Currently Amended) A method for use in a time division multiple access (TDMA) wireless subscriber unit, the method comprising:

synchronizing phase with a received signal;

operating each a plurality of circuit components in a first signal processing state having an on power consumption level, a second signal processing state having an off power consumption level, and a third signal processing state

having an intermediate power consumption level;

transitioning at least one of the plurality of circuit components among at least two of the first signal processing state, the second signal processing state, and the third signal processing state based on a time slot of a TDMA frame assigned to the TDMA wireless subscriber unit.

20. (Previously Presented) The method of claim 19, further comprising:

selecting one of a plurality of clocks for one of the plurality of circuit components based on a current one of the first signal processing state, the second signal processing state, and the third signal processing state.

21. (Previously presented) The method of claim 20, wherein the plurality of clocks is produced by a software controlled register coupled to the plurality of circuit components.

22. (Previously Presented) The method of claim 19, further comprising:

operating at least one of the plurality of circuit components in a fourth signal processing state including a reduced power sub-state.

23. (Canceled)

24. (Previously Presented) The method of claim 19, further comprising:

transitioning one of the plurality of circuit components from the third signal processing state to the first signal processing state while retaining operating state information to resume processing.

25. (Previously Presented) The method of claim 19, further comprising:

transitioning one of the plurality of circuit components from the first signal processing state to either the second signal processing state or the third signal processing state during a call connection.

26. (Previously Presented) The method of claim 19, further comprising:

selectively operating one of the plurality of circuit components in any one of the first signal processing state, the second signal processing state, and the third signal processing state responsive to a radio control channel timeslot to determine the presence of call traffic or a traffic channel assigned to the TDMA wireless subscriber unit.

27. (Canceled)

28. (Previously Presented) The method of claim 19, wherein one of the plurality of circuit components transitions between at least two power consumption levels during any single time slot.

29. (Currently Amended) A processor comprising:

a power interface circuit configured to power a plurality of circuit components, wherein each circuit component of the plurality of circuit components is configured to operate in a first signal processing state having an on power consumption level, a second signal processing state having an off power consumption level, and a third signal processing state having an intermediate

power consumption power level;

wherein at least one of the plurality of circuit components is configured to transition among at least two of the first signal processing state, the second signal processing state, and the third signal processing state based on a time slot of a TDMA frame.

30. (Previously Presented) The processor of claim 29, wherein the processor is coupled to a plurality of clocks, wherein one of the plurality of clocks is selected for one of the plurality of circuit components based on a current one of the first signal processing state, the second signal processing state, and the third signal processing state.

31. (Previously Presented) The processor of claim 30, wherein the plurality of clocks is produced by a software controlled register.

32. (Previously Presented) The processor of claim 29, wherein each circuit component of the plurality of circuit components is further configured to operate in fourth signal processing state including a reduced power sub-state.

33. (Canceled)

34. (Previously Presented) The processor of claim 29, wherein one of the plurality of circuit components is configured to retain operating state information to resume processing in response to a transition from the third signal processing state to the first signal processing state.

35. (Previously Presented) The processor of claim 29, wherein at least one of the plurality of circuit components is configured to transition from the first signal processing state to either the second signal processing state or the third signal processing state during a call connection.

36. (Previously Presented) The processor of claim 29, wherein the plurality of circuit components are configured to be selectively operated in any one of the first signal processing state, the second signal processing state, and the third signal processing state responsive to a radio control channel timeslot to determine the presence of call traffic or a traffic channel assigned to the TDMA wireless subscriber unit.

37. (Canceled)

38. (Previously Presented) The processor of claim 29, wherein the at least one of the plurality of circuit components is configured to transition among the first signal processing state, the second signal processing state, and the third signal processing state during a signal time slot.

39. (Previously Presented) The processor of claim 29, wherein at least one of the plurality of circuit components is collocated with the processor

40. (Previously Presented) The TDMA wireless subscriber unit of claim 9, wherein a first circuit component and a second circuit component of the plurality

of circuit components are configured to operate concurrently in the first and third signal processing states, respectively.

41. (Previously Presented) The TDMA wireless subscriber unit of claim 40, wherein a third circuit component of the plurality of circuit components is configured to operate in the second signal processing state concurrently with the first and second circuit components.

42. (Previously Presented) The TDMA wireless subscriber unit of claim 9, wherein a first circuit component and a second circuit component of the plurality of circuit components are configured to operate concurrently in the second and third signal processing states, respectively.

43. (Previously Presented) The TDMA wireless subscriber unit of claim 42, wherein a third circuit component of the plurality of circuit components is configured to operate in the first signal processing state concurrently with the first and second circuit components.

44. (Previously Presented) The method of claim 19, wherein a first circuit component and a second circuit component of the plurality of circuit components are configured to operate concurrently in the first and third signal processing states, respectively.

45. (Previously Presented) The method of claim 44, wherein a third circuit component of the plurality of circuit components is configured to operate in

the second signal processing state concurrently with the first and second circuit components.

46. (Previously Presented) The method of claim 19, wherein a first circuit component and a second circuit component of the plurality of circuit components are configured to operate concurrently in the second and third signal processing states, respectively.

47. (Previously Presented) The method of claim 47, wherein a third circuit component of the plurality of circuit components is configured to operate in the first signal processing state concurrently with the first and second circuit components.

48. (Previously Presented) The processor of claim 29, wherein a first circuit component and a second circuit component of the plurality of circuit components are configured to operate concurrently in the first and third signal processing states, respectively.

49. (Previously Presented) The processor of claim 48, wherein a third circuit component of the plurality of circuit components is configured to operate in the second signal processing state concurrently with the first and second circuit components.

50. (Previously Presented) The processor of claim 29, wherein a first circuit component and a second circuit component of the plurality of circuit

components are configured to operate concurrently in the second and third signal processing states, respectively.

51. (Previously Presented) The processor of claim 50, wherein a third circuit component of the plurality of circuit components is configured to operate in the first signal processing state concurrently with the first and second circuit components.

52. (New) The TDMA wireless subscriber unit of claim 9, wherein the plurality of circuit components are configured to operate in a first set of signal processing states associated with a first operating state, and in a second set of signal processing states associated with a second operating state, wherein the first set of signal processing states and the second set of signal processing states are different.

53. (New) The method of claim 19, wherein the plurality of circuit components are configured to operate in a first set of signal processing states associated with a first operating state, and in a second set of signal processing states associated with a second operating state, wherein the first set of signal processing states and the second set of signal processing states are different.

54. (New) The processor of claim 29, wherein the plurality of circuit components are configured to operate in a first set of signal processing states associated with a first operating state, and in a second set of signal processing states associated with a second operating state, wherein the first set of signal

processing states and the second set of signal processing states are different.